



OTT2001A

208-channel Capacitive Touch Sensor Driver for Passive Matrix Touch Panel

Preliminary

OCT. 30, 2013
Version 0.1

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208-CHANNEL CAPACITIVE DRIVER FOR PASSIVE MATRIX TOUCH PANEL

1. GENERAL DESCRIPTION

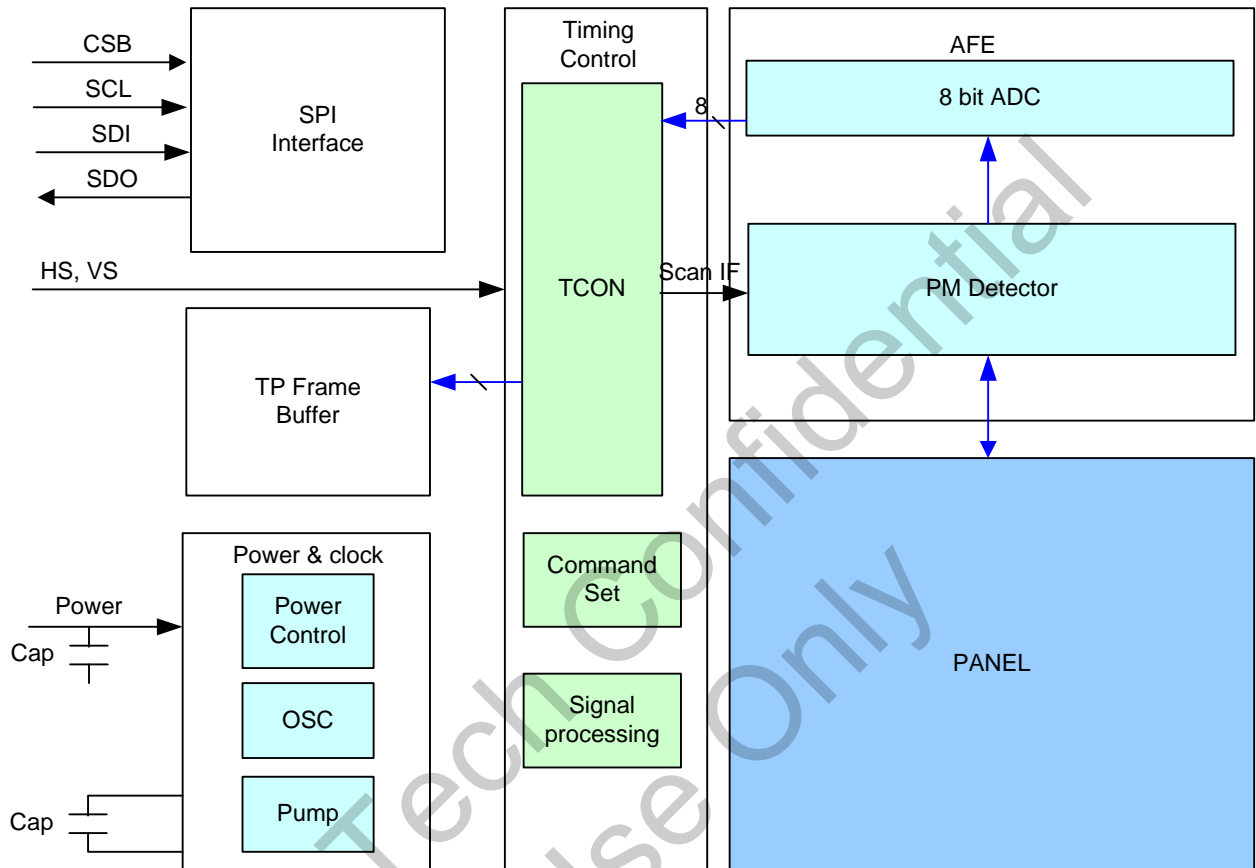
The OTT2001A, a 208 channels capacitive touch driver LSI, is designed for up to 10.1" passive matrix touch panel. It includes high speed 4 wire SPI interface to communicate with host processor, 8 bit SAR-ADC to transfer charge variation to digital code, and internal charge pump to supply 4X voltage of touch sensing unit for passive matrix touch panel. Moreover, an internal TP buffer, which can be used to store whole TP raw data, is also built in OTT2001A. The TP buffer can reduce the latency between host processor and OTT2001A.

2. FEATURES

- Supports passive matrix touch panel up to 10.1" , incorporating a 208-channel sensing drivers. Combined with display gate driver, it can provide touch sensing signal to touch electrode on PM panel.
- 8-bit SAR ADC converter to convert charge variation to digital code when human's finger touch the touch panel
- Built-in 624 (208 x 3) bytes internal SRAM as TP buffer
- System interfaces
 - 4 wire(CSX, DI, DO, CLK), high-speed interfaces, max to 15Mhz to support high speed data transfer between host processor and touch driver
- Power supply
 - I/O interface supply voltage (VDDIO): 1.8 ~ 5.5 V, typical 3.3V.
 - Analog power supply voltage (VCI): 2.8 ~ 5.5 V, typical 3.3V
- On-chip power management system
 - Power saving mode to reduce power consumption when no touched (STBY function)
- Built-in Charge Pump circuits
 - Sensing driver voltage level: VDDA-GND=8V ~ 12V.
 - Built-in internal oscillator and hardware reset
- External Component
 - 4 Capacitors for Power and Charge Pump circuits.

3. BLOCK DIAGRAM

3.1. Block Function



3.1.1. System Interface

The OTT2001A supports SPI system high-speed interfaces:

- 4-pin 8-bits Serial Peripheral Interface (SPI)

The OTT2001A has three data registers, 1) index register (IR), 2) write-data register (WDR) and 3) read-data register (RDR). The IR register is used to store index information from control registers. The WDR register is used to temporarily store data to be written for register control and internal TP buffer. The RDR register is used to temporarily store data read from the TP buffer. When touch data is written to the internal TP buffer from MCU engine, the data is first written to the WDR and then automatically written to the internal TP buffer by internal operation. When touch data read operation is executed, touch data is read via the RDR from the internal TP buffer. Therefore, invalid data is first read out to the data bus when the OTT2001A executes the 1st read operation. Thus, valid data can be read out after the OTT2001A executes the 2nd read operation.

Table 3-1 Register Selection (Serial Peripheral Interface)

Start byte (SPI)		Function
R/W	RS	
0	0	Write an index to IR
1	0	Reserved
0	1	Write into control registers and the internal TP buffer via WDR
1	1	Read from the internal TP buffer and registers via RDR

3.1.2. Address Counter (AC)

OTT2001A includes an address counter (AC) gives an address to the TP buffer. The address in the AC is automatically updated plus 1.

3.1.3. TP buffer

OTT2001A includes a TP buffer which has the capacity of 624 (208 x 3) bytes.

3.1.4. 8 bit SAR ADC

OTT2001A has a 8-bit resolution SAR A/D converter, which can transfer capacitance variance to max 256 touch scale for touch application.

3.1.5. Timing Controller

OTT2001A has a timing controller which can generates a timing signal for internal circuits operation such as sensing timing, RAM accessing timing, etc.

3.1.6. Oscillator (OSC)

The OTT2001A include an internal oscillator, which generates RC oscillation without an external resistor. The frequency can be adjusted through the register setting. In standby mode, RC oscillation is halted to reduce power consumption.

3.1.7. Sensing Circuit

OTT2001A consists of 208-output sensing circuit (C1 ~ C208). When human's fingers touch the touch panel, touch Data would be accumulated or integrated by the sensing circuit. After sensing or amplifying operation, the analog signal would be transferred to digital code by SAR ADC. Then all TP data would be stored into TP buffer.

3.1.8. Touch Power Supply Circuit

The touch power supply circuit generates the voltage levels VDRV. All this voltages can be adjusted by register setting.

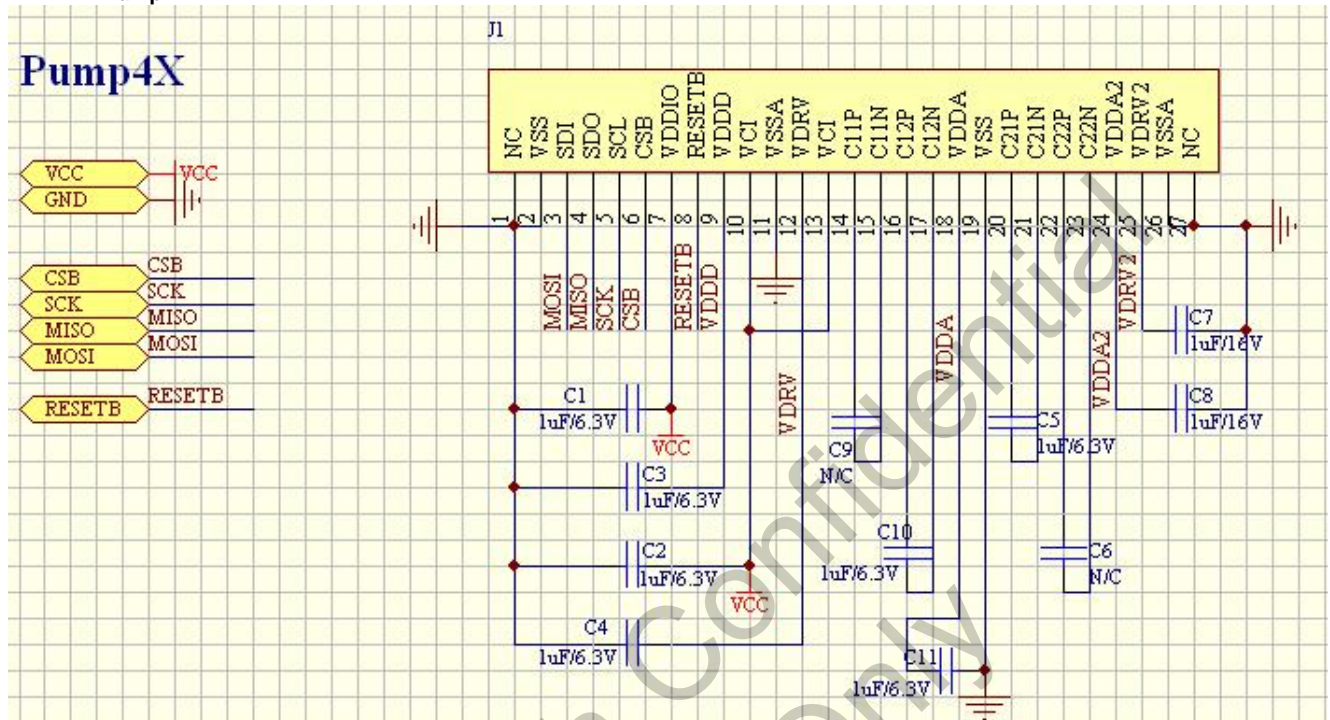
4. SIGNAL DESCRIPTIONS

4.1. Pin Definition

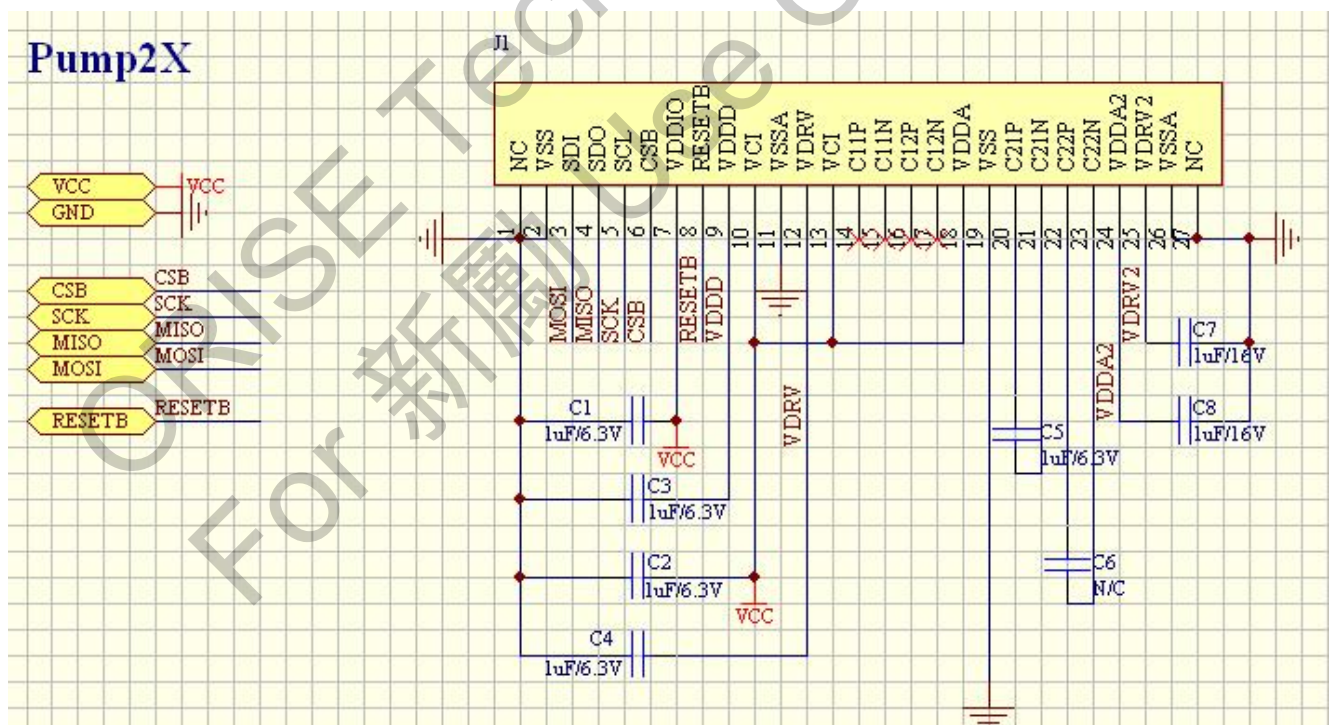
Signal	I/O	Connected with	Function
System Configuration Input Signal			
RESETB	I	MPU or external RC circuit	RESET pin. This is an active low signal.
Interface Input Signals			
CSB	I	MPU	Chip select signal. Low: the OTT2001A is accessible High: the OTT2001A is not accessible
SCL	I	MPU	Served as a synchronizing clock signal. (SCL)
SDI	I	MPU	Series Data is the input on the rising edge of the SCL signal in SPI mode.
SDO	O	MPU	Series Data is the output on the rising edge of the SCL signal in SPI mode.
VSYN	I	MPU	External sync signal.
HSYN / TE	I	MPU	External sync signal.
INT	O	MPU	Interrupt output to indicate end of operation on OTT2001A
OSC_IN	IO	MPU	External oscillator input/out pin
Charge Pump and Power Supply Signal			
C11P, C11N	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins.
C12P, C12N	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins.
C21P, C21N	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins.
C22P, C22N	-	Step-up capacitor	Connect boost capacitors for the internal DC/DC converter circuit to these pins.
VDRV	O	Stabilizing capacitor	High level voltage output of driving pulse
VDDA2	I	Stabilizing capacitor	Charge pump output voltage
VDDA	I	Stabilizing capacitor	Charge pump output voltage
VDRV2	O	Stabilizing capacitor	Internal regulator voltage output for driving circuit
Channel			
C1~C208	I/O	TP	Input/output touch signals.
Pads for Power Supplies			
VOTP	-	Power supply	Power supply for programming OTP memory
VSS	-	GND	Internal logic GND and Charge pump GND.
VDDIO	-	Power supply	Power supply to the interface pins: RESETB, CSB, SCL, SDI, SDO, VSYN, HSYN,
VSSA	-	GND	Analog GND: VSSA = 0V.
VCI	I	Power supply	Power supply to the power supply analog circuit.
Misc. Signal			
MODE[1:0]	O	Open	Test mode selection. Leave it open. Internal pull-low

4.2. Application Circuit

4.2.1. Pump4X



4.2.2. Pump2X



4.3. BOM List

4.3.1. Pump4X

OTT2001A BOM LISTS				
NO.	Signal Name	Value	Max. Ability	Note
1	VDDIO	1.0uF	6.3V	I/O Power
2	VCI	1.0uF	6.3V	Analog Power
3	VDDD	1.0uF	6.3V	Digital Power
4	VDRV	1.0uF	6.3V	VDDA Pump
5	C21P/C21N	1.0uF	6.3V	VDDA2 Pump
6	C22P/C22N	1.0uF	6.3V	VDDA2 Pump (Option)
7	VDRV2	1.0uF	16V	VDDA2 Pump
8	VDDA2	1.0uF	16V	VDDA2 Pump
9	C11P/C11N	1.0uF	6.3V	VDDA Pump (Option)
10	C12P/C12N	1.0uF	6.3V	VDDA Pump
11	VDDA	1.0uF	6.3V	VDDA Pump

4.3.2. Pump2X

OTT2001A BOM LISTS				
NO.	Signal Name	Value	Max. Ability	Note
1	VDDIO	1.0uF	6.3V	I/O Power
2	VCI	1.0uF	6.3V	Analog Power
3	VDDD	1.0uF	6.3V	Digital Power
4	VDRV	1.0uF	6.3V	VDDA Pump
5	C21P/C21N	1.0uF	6.3V	VDDA2 Pump
6	C22P/C22N	1.0uF	6.3V	VDDA2 Pump (Option)
7	VDRV2	1.0uF	16V	VDDA2 Pump
8	VDDA2	1.0uF	16V	VDDA2 Pump

5. RESET FUNCTION

The OTT2001A can be reset by hardware (/RESET pin). While /RESET is in low level (RESET period), accessing to instructions or to TP buffer data are terminated temporarily. Be sure that /RESET period must last at least 20us for RESET function to be functional. In case of power-on reset, wait at least 10ms for RC oscillation stabilization. Moreover, TP buffer data are not initialized automatically during RESET period. User should issue a clear command to make sure all TP buffer data keep at 00h.

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6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings:

Table 6-1

Item	Symbol	Value	Unit	Note
Power Supply Voltage 1	VDDIO – VSS	-0.0 ~+5.5	V	
Power Supply Voltage 2	VCI – VSS	-0.0 ~+5.5	V	
Input Voltage	Vt	-0.3 ~VDDIO + 0.3	V	
Operating Temperature	Topr	-30 ~+70	°C	
Storage Temperature	Tstg	-40 ~+85	°C	

6.2. DC Characteristics

Table 6-2

VCI=2.8V~5.50V, VDDIO=1.8V~5.50V, Ta=-30°C~+70°C

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input High level voltage	V _{IH}	V	VDDIO=1.8V~5.50V	0.7xVDDIO	-	VDDIO	
Input Low level voltage	V _{IL}	V	VDDIO=1.8V~5.50V	0	-	0.3xVDDIO	
Output "High" level voltage 1 (SDO, INT)	V _{OH}	V	VDDIO=1.8V~5.50V, I _{OH} =-0.5mA	0.8xVDDIO	-	VDDIO	
Output "Low" level voltage 1 (SDO, INT)	V _{OL}	V	VDDIO=1.8V~5.50V, I _{OH} =-0.5mA	0	-	0.2xVDDIO	
I/O leak current	I _{LI}	μA	Vin= 0 / VDDIO	-5	-	5	
Current Consumption (VDDIO-IOGND) Normal operation mode	I _{OP1}	μA	fosc=1.6MHz VDDIO=VCI=3.30V Ta=25°C	-	TBD	-	
Current Consumption (VDDIO-IOGND) Standby mode	I _{OP2}	μA	VDDIO=VCI=3.30V Ta=25°C	-	-	30	

6.3. AC Characteristics

VCI=2.8V~5.50V, VDDIO=1.8V~5.50V, Ta=-30℃~+70℃

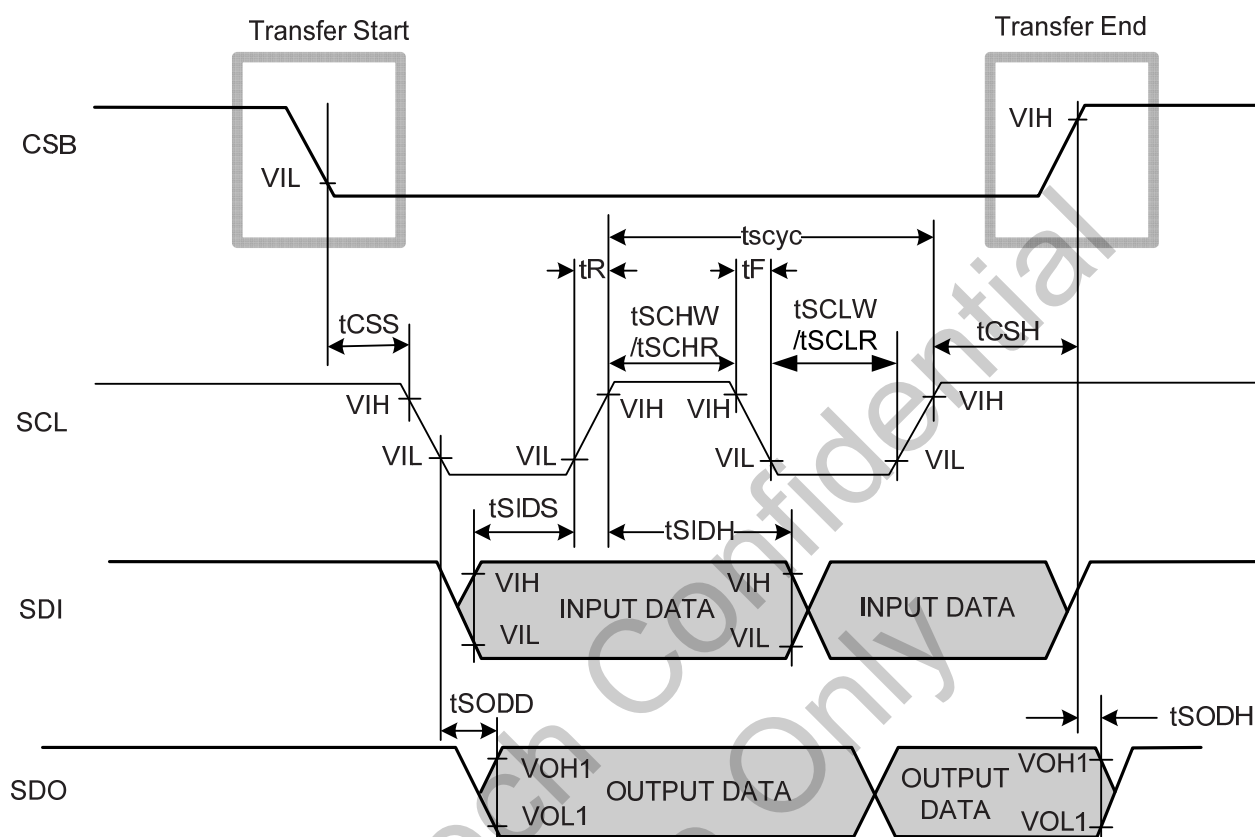
6.3.1. Clock Characteristics

Item	Symbol	Unit	Timing Diagram	Min.	Typ.	Max.	Note
RC Oscillation clock	fosc	MHz	VDDIO = VCI = 3.3V, 25℃	-	1.6	-	-

6.3.2. Clock-synchronized Serial Interface Timing Characteristics

VDDIO=1.8~5.50V

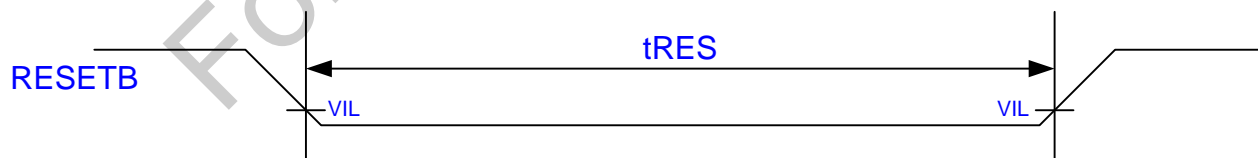
Item	Symbol	Unit	Min.	Typ.	Max.
Serial Time Clock Cycle	Write (received)	tSCYC	ns	66	-
	Read (transmitted)	tSCYC	ns	66	-
Serial Clock high-level width	Write (received)	tSCHW	ns	25	-
	Read (transmitted)	tSCHR	ns	25	-
Serial Clock low-level width	Write (received)	tSCLW	ns	25	-
	Read (transmitted)	tSCLR	ns	25	-
Serial clock rise/fall time	tR, tF	ns	-	-	10
Chip select setup time	tCSS	ns	25	-	-
Chip select hold time	tCSH	ns	25	-	-
Serial input data setup time	tSIDS	ns	20	-	-
Serial input data hold time	tSIDH	ns	20	-	-
Serial output data delay time	tSODD	ns	-	-	40
Serial output data hold time	tSODH	ns	5	-	-

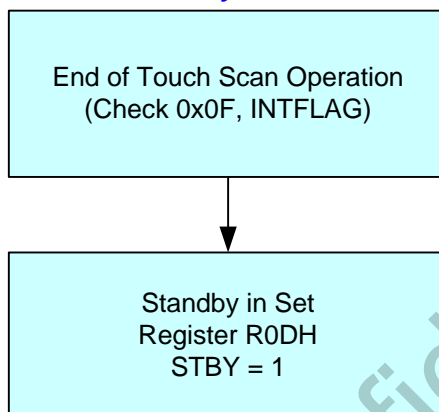
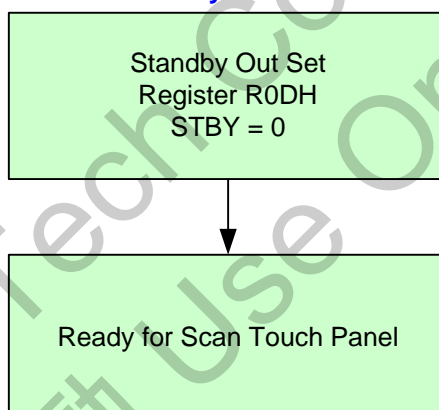


6.3.3. Reset Timing Characteristics (VDDIO=1.8~5.50V)

Table 6-3

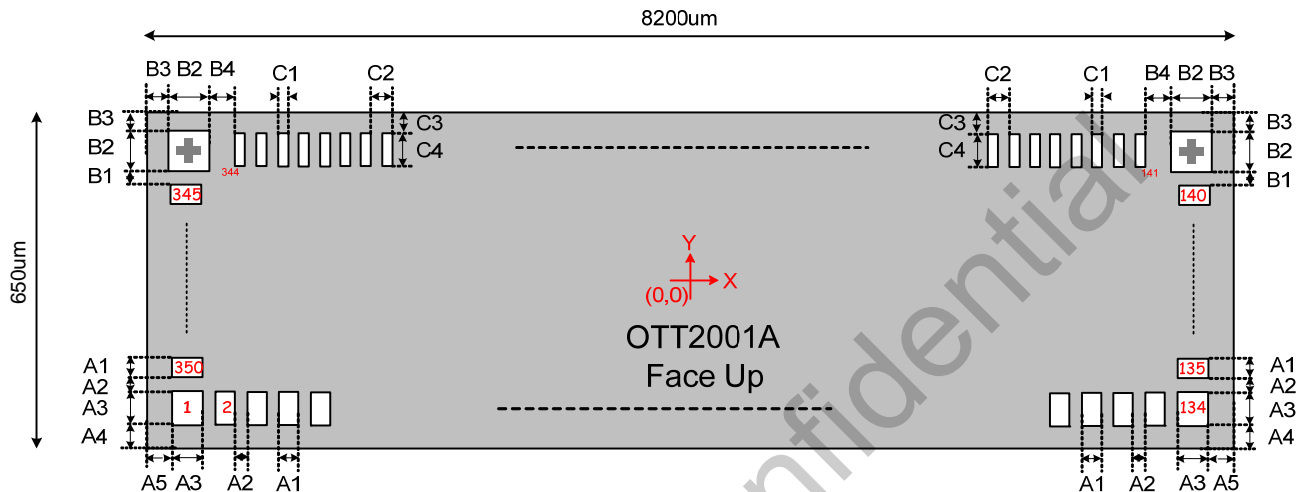
Item	Symbol	Unit	Min.	Typ.	Max.
Reset low-level width	tRES	us	20	—	—



7. POWER ON/OFF SEQUENCE**Standby in / out Sequence****Standby in flow****Standby Out flow**

8. CHIP INFORMATION (FOR COG)

8.1. PAD Assignment



Note1: Have no Temperature compensation design

Symbol	Size	Symbol	Size	Symbol	Size
A1	40	B1	15	C2	37
A2	20	B2	100	C3	55
A3	70	B3	10	C4	88
A4	55	B4	54	Unit : um	
A5	60	C1	22		

8.2. Pad Dimensions

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	8200	650	μm
Chip thickness	-	150±10		
Pad pitch	2~133 ,135~140, 345~350	60	-	
	141~344	37	-	
	1,134	75	-	
Pad size	2~133 ,135~140, 345~350	40	70	
	141~344	22	88	
	1,134	70	70	

Note1: Chip size included scribe line.

Note2: Included Pump.

8.3. PAD Locations (For COG)

NO.	PAD Name	X	Y
1	VSS	-4005	-235
2	OSC_IO	-3930	-235
3	INT	-3870	-235
4	SDI	-3810	-235
5	SDO	-3750	-235
6	SCL	-3690	-235
7	CSB	-3630	-235
8	HSYNC	-3570	-235
9	VSYNC	-3510	-235
10	MODE1	-3450	-235
11	MODE0	-3390	-235
12	VDDIO	-3330	-235
13	VDDIO	-3270	-235
14	VDDIO	-3210	-235
15	VDDIO	-3150	-235
16	RESETB	-3090	-235
17	VDDD	-3030	-235
18	VDDD	-2970	-235
19	VDDD	-2910	-235
20	VDDD	-2850	-235
21	VCI	-2790	-235
22	VCI	-2730	-235
23	VCI	-2670	-235
24	VCI	-2610	-235
25	VSSA	-2550	-235
26	VSSA	-2490	-235
27	VSSA	-2430	-235
28	VSSA	-2370	-235
29	VSSA	-2310	-235
30	VDRV	-2250	-235
31	VDRV	-2190	-235
32	VDRV	-2130	-235
33	VDRV	-2070	-235
34	VDRV	-2010	-235
35	VDRV	-1950	-235
36	VDRV	-1890	-235
37	VCI	-1830	-235
38	VCI	-1770	-235
39	VCI	-1710	-235
40	VCI	-1650	-235
41	VCI	-1590	-235
42	VCI	-1530	-235
43	VCI	-1470	-235
44	VCI	-1410	-235
45	VCI	-1350	-235
46	VCI	-1290	-235
47	VCI	-1230	-235
48	VCI	-1170	-235
49	C11P	-1110	-235
50	C11P	-1050	-235
51	C11P	-990	-235
52	C11P	-930	-235
53	C11P	-870	-235
54	C11P	-810	-235
55	C11N	-750	-235
56	C11N	-690	-235
57	C11N	-630	-235
58	C11N	-570	-235
59	C11N	-510	-235
60	C11N	-450	-235
61	C12P	-390	-235
62	C12P	-330	-235
63	C12P	-270	-235
64	C12P	-210	-235
65	C12P	-150	-235
66	C12P	-90	-235
67	C12N	-30	-235

NO.	PAD Name	X	Y
68	C12N	30	-235
69	C12N	90	-235
70	C12N	150	-235
71	C12N	210	-235
72	C12N	270	-235
73	VDDA	330	-235
74	VDDA	390	-235
75	VDDA	450	-235
76	VDDA	510	-235
77	VDDA	570	-235
78	VDDA	630	-235
79	VSS	690	-235
80	VSS	750	-235
81	VSS	810	-235
82	VSS	870	-235
83	VSS	930	-235
84	VSS	990	-235
85	VSS	1050	-235
86	VSS	1110	-235
87	VSS	1170	-235
88	VSS	1230	-235
89	VSS	1290	-235
90	VSS	1350	-235
91	VSS	1410	-235
92	VSS	1470	-235
93	VSS	1530	-235
94	VSS	1590	-235
95	C21P	1650	-235
96	C21P	1710	-235
97	C21P	1770	-235
98	C21P	1830	-235
99	C21N	1890	-235
100	C21N	1950	-235
101	C21N	2010	-235
102	C21N	2070	-235
103	C22P	2130	-235
104	C22P	2190	-235
105	C22P	2250	-235
106	C22P	2310	-235
107	C22N	2370	-235
108	C22N	2430	-235
109	C22N	2490	-235
110	C22N	2550	-235
111	VDDA2	2610	-235
112	VDDA2	2670	-235
113	VDDA2	2730	-235
114	VDDA2	2790	-235
115	VDDA2	2850	-235
116	VDDA2	2910	-235
117	VDRV2	2970	-235
118	VDRV2	3030	-235
119	VDRV2	3090	-235
120	VDRV2	3150	-235
121	VDRV2	3210	-235
122	VDRV2	3270	-235
123	VDRV2	3330	-235
124	VDRV2	3390	-235
125	VDRV2	3450	-235
126	VDRV2	3510	-235
127	VDRV2	3570	-235
128	VDRV2	3630	-235
129	VSSA	3690	-235
130	C205	3750	-235
131	C206	3810	-235
132	C207	3870	-235
133	C208	3930	-235
134	VSSA	4005	-235

NO.	PAD Name	X	Y
135	VSSA	4005	-160
136	VSSA	4005	-100
137	VSSA	4005	-40
138	VSSA	4005	20
139	VSSA	4005	80
140	VSSA	4005	140
141	C204	3885	226
142	C203	3848	226
143	C202	3811	226
144	C201	3774	226
145	C200	3737	226
146	C199	3700	226
147	C198	3663	226
148	C197	3626	226
149	C196	3589	226
150	C195	3552	226
151	C194	3515	226
152	C193	3478	226
153	C192	3441	226
154	C191	3404	226
155	C190	3367	226
156	C189	3330	226
157	C188	3293	226
158	C187	3256	226
159	C186	3219	226
160	C185	3182	226
161	C184	3145	226
162	C183	3108	226
163	C182	3071	226
164	C181	3034	226
165	C180	2997	226
166	C179	2960	226
167	C178	2923	226
168	C177	2886	226
169	C176	2849	226
170	C175	2812	226
171	C174	2775	226
172	C173	2738	226
173	C172	2701	226
174	C171	2664	226
175	C170	2627	226
176	C169	2590	226
177	C168	2553	226
178	C167	2516	226
179	C166	2479	226
180	C165	2442	226
181	C164	2405	226
182	C163	2368	226
183	C162	2331	226
184	C161	2294	226
185	C160	2257	226
186	C159	2220	226
187	C158	2183	226
188	C157	2146	226
189	C156	2109	226
190	C155	2072	226
191	C154	2035	226
192	C153	1998	226
193	C152	1961	226
194	C151	1924	226
195	C150	1887	226
196	C149	1850	226
197	C148	1813	226
198	C147	1776	226
199	C146	1739	226
200	C145	1702	226
201	C144	1665	226

NO.	PAD Name	X	Y
202	C143	1628	226
203	C142	1591	226
204	C141	1554	226
205	C140	1517	226
206	C139	1480	226
207	C138	1443	226
208	C137	1406	226
209	C136	1369	226
210	C135	1332	226
211	C134	1295	226
212	C133	1258	226
213	C132	1221	226
214	C131	1184	226
215	C130	1147	226
216	C129	1110	226
217	C128	1073	226
218	C127	1036	226
219	C126	999	226
220	C125	962	226
221	C124	925	226
222	C123	888	226
223	C122	851	226
224	C121	814	226
225	C120	777	226
226	C119	740	226
227	C118	703	226
228	C117	666	226
229	C116	629	226
230	C115	592	226
231	C114	555	226
232	C113	518	226
233	C112	481	226
234	C111	444	226
235	C110	407	226
236	C109	370	226
237	C108	333	226
238	C107	296	226
239	C106	259	226
240	C105	222	226
241	C104	185	226
242	C103	148	226
243	C102	-148	226
244	C101	-185	226
245	C100	-222	226
246	C99	-259	226
247	C98	-296	226
248	C97	-333	226
249	C96	-370	226
250	C95	-407	226
251	C94	-444	226
252	C93	-481	226
253	C92	-518	226

NO.	PAD Name	X	Y
254	C91	-555	226
255	C90	-592	226
256	C89	-629	226
257	C88	-666	226
258	C87	-703	226
259	C86	-740	226
260	C85	-777	226
261	C84	-814	226
262	C83	-851	226
263	C82	-888	226
264	C81	-925	226
265	C80	-962	226
266	C79	-999	226
267	C78	-1036	226
268	C77	-1073	226
269	C76	-1110	226
270	C75	-1147	226
271	C74	-1184	226
272	C73	-1221	226
273	C72	-1258	226
274	C71	-1295	226
275	C70	-1332	226
276	C69	-1369	226
277	C68	-1406	226
278	C67	-1443	226
279	C66	-1480	226
280	C65	-1517	226
281	C64	-1554	226
282	C63	-1591	226
283	C62	-1628	226
284	C61	-1665	226
285	C60	-1702	226
286	C59	-1739	226
287	C58	-1776	226
288	C57	-1813	226
289	C56	-1850	226
290	C55	-1887	226
291	C54	-1924	226
292	C53	-1961	226
293	C52	-1998	226
294	C51	-2035	226
295	C50	-2072	226
296	C49	-2109	226
297	C48	-2146	226
298	C47	-2183	226
299	C46	-2220	226
300	C45	-2257	226
301	C44	-2294	226
302	C43	-2331	226
303	C42	-2368	226
304	C41	-2405	226
305	C40	-2442	226

NO.	PAD Name	X	Y
306	C39	-2479	226
307	C38	-2516	226
308	C37	-2553	226
309	C36	-2590	226
310	C35	-2627	226
311	C34	-2664	226
312	C33	-2701	226
313	C32	-2738	226
314	C31	-2775	226
315	C30	-2812	226
316	C29	-2849	226
317	C28	-2886	226
318	C27	-2923	226
319	C26	-2960	226
320	C25	-2997	226
321	C24	-3034	226
322	C23	-3071	226
323	C22	-3108	226
324	C21	-3145	226
325	C20	-3182	226
326	C19	-3219	226
327	C18	-3256	226
328	C17	-3293	226
329	C16	-3330	226
330	C15	-3367	226
331	C14	-3404	226
332	C13	-3441	226
333	C12	-3478	226
334	C11	-3515	226
335	C10	-3552	226
336	C9	-3589	226
337	C8	-3626	226
338	C7	-3663	226
339	C6	-3700	226
340	C5	-3737	226
341	C4	-3774	226
342	C3	-3811	226
343	C2	-3848	226
344	C1	-3885	226
345	VOTP	-4005	140
346	VSS	-4005	80
347	VSS	-4005	20
348	VSS	-4005	-40
349	VSS	-4005	-100
350	VSS	-4005	-160

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10. REVISION HISTORY

Date	Revision #	Description	Page	Auditor
OCT. 30, 2013	0.2	Modify 8.2 Pad Dimensions	14	Berton.Huang
JUN. 28, 2013	0.1	Original	19	Berton.Huang

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