Data Sheet

Core1081

Embedded Wi-Fi module

2.2 **Date：2014-02-13** **Data Sheet**

Overview

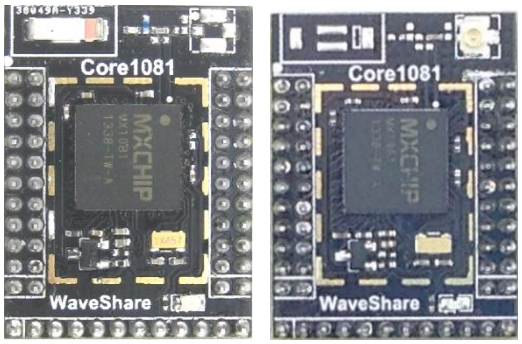
Core1081 is an ultra-compact, low-power embedded Wi-Fi module based on MX1081, a fully integrated System-on-Chip that is fully compatible with Broadcom WICED platform. MX1081 integrates a wireless LAN MAC/baseband/radio, and a Cortex-M3 microcontroller STM32F205 that runs a unique "self-hosted" Wi-Fi networking library and software application stack. Core1081 has 1M bytes flash, 128k RAM and rich peripherals for your embedded Wi-Fi applications.

Core1081 is also anmxchipWNetTMcompatible platform, users can build their own embedded Wi-Fi applications based on mxchipWNetTM library which manage all of the Wi-Fi MAC and TCP/IP stack processing. We also provide several mxchipWNetTM firmware to meet typical applications:wireless UART, wireless audio, wireless sensor etc.

When using mxchipWNetTM-DTU firmware, you can establish Wi-Fi networking for any device with a micro-controller and a UART interface. Quick development cycles enables fast time to market.

Applications

- Building Automation / Access Control
- Smart home appliances
- Medical/Health Care
- Industrial Automation Systems
- Point Of Sale system (POS)
- Auto electronics

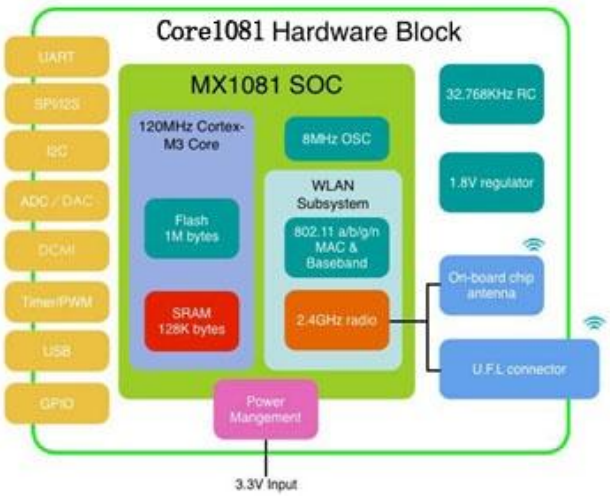


Product list

Module	-	Antenna	
Core1081	-	C	On-board chip antenna
	-	E	IPEX connector

Firmware/Library	Function
mxchipWNet™ -DTU	Predefined firmware:UART/Wi-Fi conversion
mxchipWNet™ Library	Software library used to develop custom firmware
mxchipWNet™ Library Plus	Software library based on RTOS

Hardware block



MXCHIP Co., Ltd

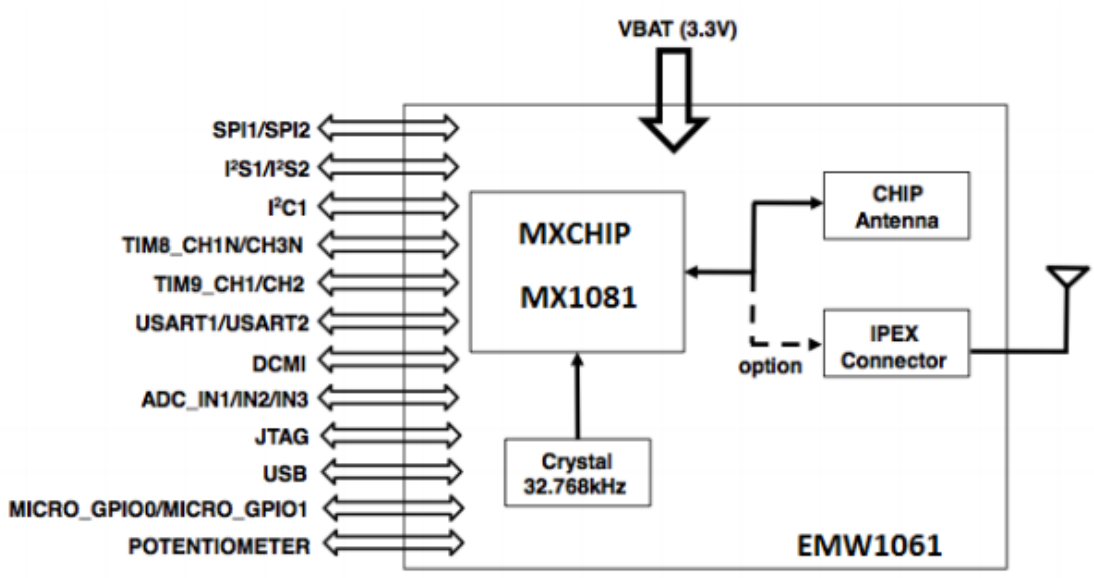
contents

1. Introduction

Core1081 is an ultra-compact, low-power embedded Wi-Fi module based on MX1080, a fully integrated System-on-Chip that is fully compatible with Broadcom WICED platform. MX1081 integrates a Broadcom BCM43362 wireless LAN MAC/baseband/radio, and an embedded processor core that runs a unique "self-hosted" Wi-Fi networking library and software application stack. Core1081 has 1M bytes flash, 128k RAM and rich peripherals for your embedded Wi-Fi applications.

Core1081 is also an **mxchipWNet™** compatible platform, users can build their own embedded Wi-Fi applications based on **mxchipWNet™** library which manage all of the Wi-Fi MAC and TCP/IP stack processing. We also provide several mxchipWNetTM firmware to meet typical applications: wireless UART, wireless audio, wireless sensor etc.

When using **mxchipWNet™**-DTU firmware, you can establish Wi-Fi networking for any device with a micro-controller and a serial interface. Quick development cycles enables fast time to market.



1.1. Features

- Single operation voltage：3.3V
- Power consumption:
  Only ~7mA while module is connected to access point and no data is transmitting,
  Only ~24mA while sending data under 20kbps,
  Only 8μA under standby mode.
- STM32F2 MCU frequency: 120MHz，flash size: 1M bytes，RAM size: 128k bytes.
- On-chip functionality Single-chip: MAC/BB/RF
- Peripherals：
  - 42 x GPIOs
  - 3 x UARTs，UART2 include hardware flow control
  - 2 x SPI, 1xIIS
  - 8 x ADC input channels，2 DAC output channel
  - 1 x USB device, 1 x CAN
  - 2 x I2C
  - PWM/Timer input/output
  - DCMI
  - SWD debug interface
- Wi-Fi connectivity
  - 802.11b, 802.11g, 802.11n (single stream) on channel 1-14@2.4GHz
  - WEP, WPA/WPA2 PSK/Enterprise
  - Transmit power：18.5dBm@11b，15.5dBm@11g，14.5dBm@11n
  - MIN Receiver Sensitivity: -96 dBm
  - Max Data rate：11Mbps@11b，54Mbps@11g，72Mbps@11n HT20
  - Wi-Fi modes：Station, Soft AP and Wi-Fi direct
  - Advanced 1x1 802.11n features
    Full/Half Guard Interval
    Frame Aggregation
    Space Time Block Coding (STBC)
    Low Density Parity Check (LDPC) Encoding
  - Hardware Encryption: WEP, WPA/WPA2
  - WPS 2.0
  - Multiple power save modes
  - On-board chip antenna，IPEX connector for external antenna
  - CE，FCC compliant
- Operating Temperature: -40℃ to 85℃
- MSL level 3

2. Interface

2.1. Pinouts

Core1081 has Three groups of pins . The lead pitch is 2mm.

Core1081 pinout is shown in the Figure 2.1. Table 2.2 lists the pin functions.

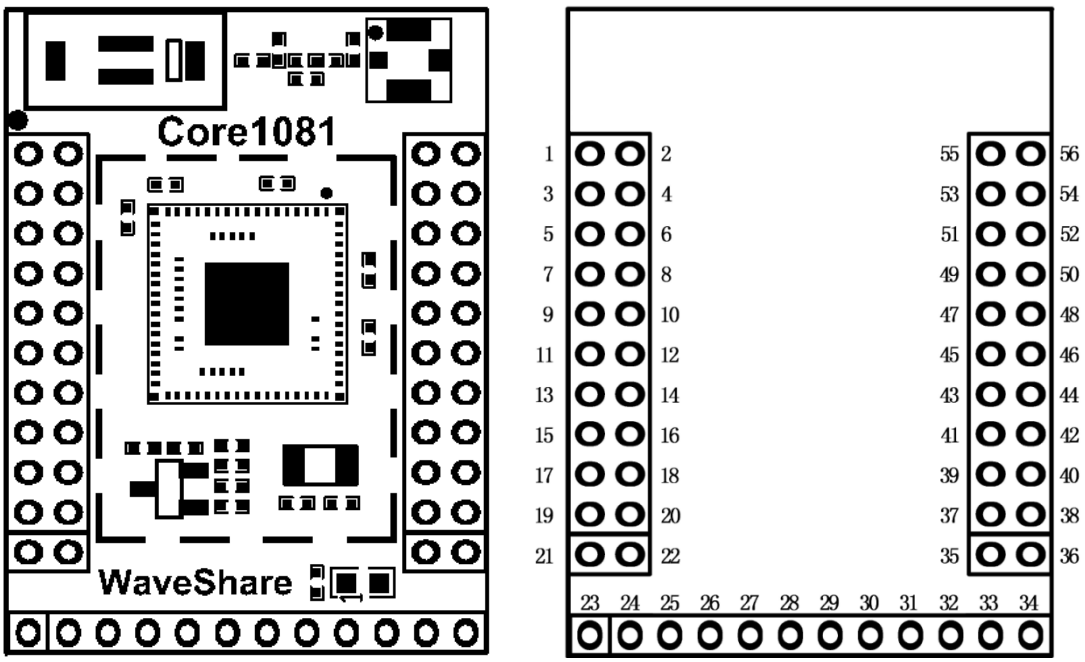


Figure2.1 Core1081: appearance and pinout

2.2. Pin Arrangement

Figure 2.2 Core1081 pin arrangement

Pins Number	Pin Name	Type	IO level	Main function (after reset)	Alternate functions	Other functions
1	PA6	I/O	FT	PA6	SPI1_MISO / TIM8_BKIN/TIM13_CH1 / DCMI_PIXCLK / TIM3_CH1 / TIM1_BKIN/ EVENTOUT	ADC12_IN6
2	PA7	I/O	FT	PA7	SPI1_MOSI/ TIM8_CH1N / TIM14_CH1 TIM3_CH2/ ETH_MII_RX_DV / TIM1_CH1N / RMII_CRS_DV / EVENTOUT	ADC12_IN7
3	PB15	I/O	FT	PB15	SPI2_MOSI / I2S2_SD / TIM1_CH3N / TIM8_CH3N / TIM12_CH2 / OTG_HS_DP / RTC_50Hz/ EVENTOUT	
4	PB14	I/O	FT	PB14	SPI2_MISO/ TIM1_CH2N / TIM12_CH1 / OTG_HS_DM USART3_RTS/ TIM8_CH2N/ EVENTOUT	
5	PB12	I/O	FT	PB12	SPI2_NSS/I2S2_WS/ I2C2_SMBA/ USART3_CK/ TIM1_BKIN / CAN2_RX / OTG_HS_ULPI_D5/ ETH_RMII_TXD0 / ETH_MII_TXD0/ OTG_HS_ID/ EVENTOUT	
6	PH8	I/O	FT	PH8	I2C3_SDA / DCMI_HSYNC/ EVENTOUT	
7	PH9	I/O	FT	PH9	I2C3_SMBA / TIM12_CH2/ DCMI_D0/ EVENTOUT	
8	PH10	I/O	FT	PH10	TIM5_CH1 / DCMI_D1/ EVENTOUT	
9	PH11	I/O	FT	PH11	TIM5_CH2 / DCMI_D2/ EVENTOUT	

Pins Number	Pin Name	Type	IO level	Main function (after reset)	Alternate functions	Other functions
10	PH12	I/O	FT	PH12	TIM5_CH3 / DCMI_D3/ EVENTOUT	
11	PH14	I/O	FT	PH14	TIM8_CH2N / DCMI_D4/ EVENTOUT	
12	PA9	I/O	FT	PA9	USART1_TX/ TIM1_CH2 / I2C3_SMBA / DCMI_D0/ EVENTOUT	OTG_FS_ VBUS
13	PA10	I/O	FT	PA10	USART1_RX/ TIM1_CH3/ OTG_FS_ID/DCMI_D1/ EVENTOUT	
14	PD0	I/O	FT	PD0	FSMC_D2/CAN1_RX/ EVENTOUT	
15	PD1	I/O	FT	PD1	FSMC_D3 / CAN1_TX/ EVENTOUT	
16	PD5	I/O	FT	PD5	FSMC_NWE/USART2_TX/ EVENTOUT	
17	PD6	I/O	FT	PD6	FSMC_NWAIT/ USART2_RX/ EVENTOUT	
18	PA13	I/O	FT	PA13	JTMS-SWDIO/ EVENTOUT	
19	PA14	I/O	FT	PA14	JTCK-SWCLK/ EVENTOUT	
20	PA15	I/O	FT	PA15	JTDI/ SPI3_NSS/ I2S3_WS/TIM2_CH1_ETR / SPI1_NSS/ EVENTOUT	
21	PB3	I/O	FT	PB3	JTDO/ TRACESWO/ SPI3_SCK / I2S3_SCK / TIM2_CH2 / SPI1_SCK/ EVENTOUT	
22	PB4	I/O	FT	PB4	NJTRST/ SPI3_MISO / TIM3_CH1 / SPI1_MISO/ EVENTOUT	
23	GND			GND		
24	3.3V			3.3V		
25	PH13	I/O	FT	PH13	TIM8_CH1N / CAN1_TX/ EVENTOUT	
26	PH15	I/O	FT	PH15	TIM8_CH3N / DCMI_D11/ EVENTOUT	
27	PI2	I/O	FT	PI2	TIM8_CH4 /SPI2_MISO / DCMI_D9/ EVENTOUT	
28	PI0	I/O	FT	PI0	TIM5_CH4 / SPI2_NSS / I2S2_WS / DCMI_D13/ EVENTOUT	

Pins Number	Pin Name	Type	IO level	Main function (after reset)	Alternate functions	Other functions
29	PB7	I/O	FT	PB7	I2C1_SDA / FSMC_NL(8)/ DCMI_VSYNC / USART1_RX/ TIM4_CH2/ EVENTOUT	
30	PB6	I/O	FT	PB6	I2C1_SCL/ TIM4_CH1 / CAN2_TX / DCMI_D5/USART1_TX/ EVENTOUT	
31	PC6	I/O	FT	PC6	I2S2_MCK / TIM8_CH1/SDIO_D6 / USART6_TX / DCMI_D0/TIM3_CH1/ EVENTOUT	
32						
33	3.3V			3.3V		
34	GND			GND		
35	PI1	I/O	FT	PI1	SPI2_SCK / I2S2_SCK / DCMI_D8/ EVENTOUT	
36	BOOT0	I/O		BOOT0		
37	PI6	I/O	FT	PI6	TIM8_CH2 / DCMI_D6/ EVENTOUT	
38	PI4	I/O	FT	PI4	TIM8_BKIN / DCMI_D5/ EVENTOUT	
39	PI3	I/O	FT	PI3	TIM8_ETR / SPI2_MOSI / I2S2_SD / DCMI_D10/ EVENTOUT	
40	PI5	I/O	FT	PI5	TIM8_CH1 / DCMI_VSYNC/ EVENTOUT	
41	PI7	I/O	FT	PI7	TIM8_CH3 / DCMI_D7/ EVENTOUT	
42	PE5	I/O	FT	PE5	TRACED2 / FSMC_A21 / TIM9_CH1 / DCMI_D6/ EVENTOUT	
43	PE6	I/O	FT	PE6	TRACED3 / FSMC_A22 / TIM9_CH2 / DCMI_D7/ EVENTOUT	
44	PF9	I/O	FT	PF9	TIM14_CH1 / FSMC_CD/ EVENTOUT	ADC3_IN7

Pins Number	Pin Name	Type	IO level	Main function (after reset)	Alternate functions	Other functions
45	PF1	I/O	FT	PF1	FSMC_A1 / I2C2_SCL/ EVENTOUT	
46	PF0	I/O	FT	PF0	FSMC_A0 / I2C2_SDA/ EVENTOUT	
47	RESET	I/O		RESET		
48	PA5	I/O	TT	PA5	SPI1_SCK/ OTG_HS_ULPI_CK / TIM2_CH1_ETR/ TIM8_CHIN/ EVENTOUT	
49	PA4	I/O	TT	PA4	SPI1_NSS / SPI3_NSS / USART2_CK / DCMI_HSYNC / OTG_HS_SOF/ I2S3_WS/ EVENTOUT	
50	PB10	I/O	FT	PB10	SPI2_SCK/ I2S2_SCK/ I2C2_SCL / USART3_TX / OTG_HS_ULPI_D3 / ETH_MII_RX_ER / TIM2_CH3/ EVENTOUT	
51		I/O				
52		I/O				
53	PA0	I/O	FT	PA0	USART2_CTS/ UART4_TX/ ETH_MII_CRS / TIM2_CH1_ETR/ TIM5_CH1 / TIM8_ETR/ EVENTOUT	ADC123_IN0/ WKUP
54	PA1	I/O	FT	PA1	USART2_RTS / UART4_RX/ ETH_RMII_REF_CLK / ETH_MII_RX_CLK / TIM5_CH2 / TIM2_CH2/ EVENTOUT	ADC123_IN1
55	PA2	I/O	FT	PA2	USART2_TX/TIM5_CH3 / TIM9_CH1 / TIM2_CH3 / ETH_MDIO/ EVENTOUT	ADC123_IN2
56	PA3	I/O	FT	PA3	USART2_RX/TIM5_CH4 / TIM9_CH2 / TIM2_CH4 / OTG_HS_ULPI_D0 / ETH_MII_COL/ EVENTOUT	ADC123_IN3

1. FT = 5 V tolerant;TT = 3.6 V tolerant.

2. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
3. I = input, O = output, S = supply.
4. STM32 peripherals are not listed if they cannot be presented on current pins

2.3. Pin Arrangement for peripherals

Some of STM32 peripherals are not listed if their main function is not usable on Core1081.

USART1(AF7)				USART2(AF7)								USART4(AF8)			
TX		RX		TX		RX		CTS		RTS		CK		TX		RX	
12	PA9	13	PA10	55	PA2	56	PA3	53	PA0	54	PA1	49	PA4	53	PA0	54	PA1
30	PB6	29	PB7	16	PD5	17	PD6										

I2C1(AF4)				I2C2(AF4)					
SCL		SDA		SCL		SDA		SMBA	
30	PB6	29	PB7	45	PF1	46	PF0	5	PB12
				50	PB10				

SPI1(AF5)								SPI2(AF5)							
NSS		SCK		MISO		MOSI		NSS		SCK		MOSI		MISO	
49	PA4	48	PA5	1	PA6	2	PA7	28	PI0	35	PI1	39	PI3	27	PI2
								5	PB12	50	PB10	3	PB15	4	PB14

IIS2(AF5)							
WS		SCK		SD		MCK	
28	PI0	35	PI1	39	PI3	31	PC6
5	PB12	50	PB10	3	PB15		

CAN2(AF9)			
TX		RX	
30	PB6	5	PB12

USB_HS(AF12)					
DP		DM		ID	
3	PB15	4	PB14	5	PB12

DCMI(AF13)																							
HSYNC		PIXCK		VSYNC		D0		D1		D2		D3		D4		D5		D6		D7			
49	PA4	1	PA6	29	PB7	7	PH9	8	PH10	9	PH11	14	PH12	11	PH14	38	PI4	37	PI6	41	PI7		
6	PH8			40	PI5	12	PA9	13	PA10							30	PB6	42	PE5	43	PE6		
						31	PC6																

ADC123(AF14)								ADC12(AF14)								ADC3(AF14)	
IN0		IN1		IN2		IN3		IN4		IN5		IN6		IN7		IN7	
53	PA0	46	PA1	55	PA2	56	PA3	49	PA4	48	PA5	1	PA6	2	PA7	44	PF9

DAC1(AF14)		DAC2(AF14)	
OUT		OUT	
49	PA4	48	PA5

3. Electrical Parameters

3.1. Absolute maximum ratings:

3.1.1. Voltage & Current

Stresses above the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	Voltage	–0.3	4.0	V
V_{IN}	Input voltage on five volt tolerantpin	V_{SS}–0.3	5.5	V
V_{IN}	Input voltage on any other pin	V_{SS}–0.3	V_{DD}+0.3	V

Symbol	Ratings	Max	Unit
I_{VDD}	Total current into VDD power lines (source)	320	mA
I_{VSS}	Total current out of VSS ground lines (sink)	320	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	

3.2. Operating conditions

3.2.1. Voltage & Current

Symbol	Note	Conditions	Specification			
			Min.	Typical	Max.	Unit
V_{DD}	Voltage		2.4	3.3	3.5	V

WLAN Subsystem

Symbol	Note	Conditions	Typical	Unit
I_{RF}	OFF[1]		2	μA
I_{RF}	SLEEP[4]		200	μA
I_{RF}	Rx(Listen)[2]		52	mA
I_{RF}	Rx(Active)[3]		59	mA
I_{RF}	Power Save[5,6]		1.9	mA
I_{RF}	Tx CCK[7,10]	11 Mbps at 18.5 dBm	320	mA
I_{RF}	Tx OFDM[8,10]	54 Mbps at 15.5 dBm	270	mA
I_{RF}	Tx OFDM[9,10]	65 Mbps at 14.5 dBm	260	mA

Note 1: Power is off.

Note 2: Carrier Sense (CCA) when no carrier present

Note 3: Carrier Sense (CS) detect/Packet Rx

Note 4: Intra-beacon Sleep

Note 5: Beacon Interval = 102.4ms, DTIM = 1, Beacon duration = 1 ms @1 Mbps.

Integrated Sleep + wakeup + Beacon Rx current over 1 DTIM interval.

Note 6: In WLAN power-saving mode, the following blocks are powered down: Crystal oscillator, Baseband PLL,AFE, RF PLL, Radio

Note 7: CCK power at chip port. Duty cycle is 100%. Includes PA contribution.

Note 8: OFDM power at chip port. Duty cycle is 100%. Includes PA contribution.

Note 9: OFDM power at chip port is 16 dBm, duty cycle is 100%, includes PA contribution.

Note 10: Absolute junction temperature limits maintained through active thermal monitoring and dynamic Tx duty cycle limiting.

Microcontroller Subsystem

Typical and maximum current consumption in Run mode, code with data processing running from Flash memory (ART accelerator enabled) or RAM

Symbol	Conditions	f_{HCLK}	Running Mode	Sleep Mode	Unit
			T_A=25°C	T_A=25°C	
I_{MCU}	External clock, all peripherals enabled	120MHz	49	38	mA
		90MHz	38	30	
		60MHz	26	20	
		30MHz	14	11	
		25MHz	11	8	
		16MHz	8	6	
		8MHz	5	3.6	
		4MHz	3	2.4	
		2MHz	2	1.9	
	External clock, all peripherals disabled	120MHz	21	8	
		90MHz	17	7	
		60MHz	12	5	
		30MHz	7	3.5	
		25MHz	5	2.5	
		16MHz	4	2.1	
		8MHz	2.5	1.7	
		4MHz	2	1.5	
		2MHz	1.6	1.4	

Typical and maximum current consumptions in Stop mode

Symbol	Parameter	Conditions	Typ	Max	Unit
			T_A=25°C	T_A=25°C	
I_{MCU}	Supply current in Stop mode with main regulator in Run mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog).	0.55	1.2	mA
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog).	0.5	1.2	
	Supply current in Stop mode with main regulator in Low Power mode	Flash in Stop mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog).	0.35	1.1	
		Flash in Deep power down mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog).	0.3	1.1	

Typical and maximum current consumptions in Standby mode

Symbol	Parameter	Conditions	Typ T_A=25°C	Unit
I_{MCU}	Supply current in Standby mode	Backup SRAM ON, low-speed oscillator and RTC ON	4.0	μA
		Backup SRAM OFF, low-speed oscillator and RTC ON	3.3	
		Backup SRAM ON, RTC OFF	3.0	
		Backup SRAM OFF, RTC OFF	2.2	

Power consumption in typical operation modes[3]

Symbol	Parameter	Conditions	Min T_A=25°C	Average T_A=25°C	Max T_A=25°C	Unit
I_{module}	Total power consumption on Core1081 module	No Wi-Fi data is transmitting[1]	2.8	4.8	69.5	mA
		Receive data in UDP mode, 20k bps[1]	2.8	12	262	mA
		Send data in UDP mode, 20k bps[1]	3	24	280	mA
		RF off, MCU enter standby mode[2]	4	6	8	μA
		Connecting to AP	52	74	320	mA

Note1:TA=25°C, MCU frequency=120MHz, with data processing running from Flash memory (ART accelerator enabled). Firmware process TCP/IP stack and IEEE 802.11 MAC every 250 milliseconds, enter stop mode when no task is pending.

RF subsystem is connected to an access point and run under power save mode in IEEE 802.11n@14.5 dBm Tx power. AP Beacon Interval = 102.4ms, DTIM = 1.

Note2: Wi-Fi connection is disconnected.

Note3: These data may not be the same depend on different firmware functions.

3.3. Digital I/O port characteristics

3.3.1. Output voltage levels

Symbol	Note	Parameter	Conditions	Min.	Max.	Unit
V_{OL}	UART& IO output voltage	Output low levelvoltage	I_{IO}= +8 mA 2.7 V < VDD < 3.6 V		0.4	V
V_{OH}		Output high level voltage		V_{DD}-0.4		V
V_{OL}		Output low level voltage	I_{IO}= +20 mA 2.7 V < VDD < 3.6 V		1.3	V
V_{OH}		Output high level voltage		V_{DD}-1.3		V

3.3.2. Output voltage levels

Symbol	Note	Parameter	Conditions	Min.	Max.	Unit
V_{IL}	UART& IO input voltage	Input low level voltage	TTLlevel	-0.5	0.8	V
V_{IH}		Input high level voltage		2	VDD+0.5	V
		Input high level voltage (5V input tolerant)		2	5.5	V
V_{IL}		Input low level voltage	CMOS level	-0.5	0.35VDD	V
V_{IH}		Input high level voltage		0.65VDD	VDD+0.5	V

3.3.3. nRESET pin characteristics

The nRESET pin input driver uses CMOS technology. Core1081 contains RC (resistance-capacitance) reset circuit which ensures the module reset accurately when it powers up. If you need to reset manually, just connect the external control signals to the reset pins directly, but the control signal should be Open Drain Mode。

Symbol	Item	Conditions	Min.	Typical	Max.	Unit
$V_{IL(NRST)}$	nRESETinput low level		–0.5		0.8	V
$V_{IH(NRST)}$	nRESETinput high level		2		VDD+0.5	
R_{PU}	Resistor for Pulling up	V_{IN}= VSS	7.5	8	8.3	kΩ
C_{PD}	Capacitor for charging andResetting			100	1000	pF

3.4. Other MCU electrical parameters

Please refer to STM32F215RGT6 data sheet.

3.5. Temperature andHumidity

Symbol	Ratings	Max	Unit
T_{STG}	Storage temperature	–55 to +125	℃
T_A	Working temperature	-40 to +85	℃
Humidity	Non condensing, relative humidity	Max. 95%	

3.6. ESD

Absolute maximum ratings: The Electromagnetic Environment Electrostatic discharge

Symbol	Ratings	Conditions	Class	Max	Unit
V_{ESD}(HBM)	Electrostatic discharge voltage (human body model)	TA= +25 °C conforming to JESD22-A114	2	2000	V
V_{ESD}(CDM)	Electrostatic discharge voltage (charge device model)	TA = +25 °C conforming to JESD22-C101	II	500	

3.7. Static latch-up

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Symbol	Parameter	Class	Class
LU	Static latch-up class	TA= +105 °C conforming to JESD78A	II level A

3.8. RF characteristics

3.8.1. Basic RF characteristics

Item	Specification
Operating Frequency	2.412~2.484GHz
Wi-Fi Standard	802.11b/g/n(single stream n)
ModulationType	11b: DBPSK, DQPSK,CCK for DSSS 11g: BPSK, QPSK, 16QAM, 64QAM for OFDM 11n: MCS0~7,OFDM *
Data Rates	11b:1, 2, 5.5 and 11Mbps 11g:6, 9, 12, 18, 24, 36, 48 and 54 Mbps 11n: MCS0~7, up to 72Mbps
Antenna type	One U.F.L connector for external antenna PCB printed ANT (Reserve)

3.8.2. IEEE802.11bmode

Item	Specification
Modulation Type	DSSS / CCK
Frequency range	2400MHz~2484MHz
Channel	CH1 to CH14
Data rate	1, 2, 5.5, 11Mbps

TX Characteristics	Min.	Typical	Max.	Unit
Transmitter Output Power				
11bTarget Power		18.5		dBm
Spectrum Mask @ target power				
fc +/-11MHz to +/-22MHz			-30	dBr
fc > +/-22MHz			-50	dBr
Frequency Error	-20		+ 20	ppm
Constellation Error(peak EVM)@ target power				
1~11Mbps		-17	-10	

RX Characteristics	Min.	Typical	Max.	Unit
Minimum Input Level Sensitivity				
1Mbps (FER≦8%)		-97	-83	dBm
2Mbps (FER≦8%)		-93	-80	dBm
5.5Mbps (FER≦8%)		-91	-79	dBm
11Mbps (FER≦8%)		-89	-76	dBm
Maximum Input Level (FER≦8%)	-10			dBm

3.8.3. IEEE802.11gmode

Item	Specification
Modulation Type	OFDM
Frequency range	2400MHz~2484MHz
Channel	CH1 to CH14
Data rate	6, 9, 12, 18, 24, 36, 48, 54Mbps

TX Characteristics	Min.	Typical	Max.	Unit
Transmitter Output Power				
11gTarget Power		15.5		dBm
Spectrum Mask @ target power				
fc +/-11MHz			-20	dBr
fc +/-20MHz			-28	dBr
fc > +/-30MHz			-40	dBr
Frequency Error	-20		+ 20	ppm
Constellation Error(peak EVM)@ target power				
6Mbps			-5	dB
9Mbps			-8	dB
12Mbps			-10	dB
18Mbps			-13	dB
24Mbps			-16	dB
36Mbps			-19	dB
48Mbps			-22	dB
54Mbps		-30	-25	dB
Transmit spectrum mask				
@ 11MHz			-20	dBr
@ 20MHz			-28	dBr
@ 30MHz			-40	dBr

RX Characteristics	Min.	Typical	Max.	Unit
Minimum Input Level Sensitivity				
6Mbps (FER≦10%)		-90	-82	dBm
9Mbps (FER≦10%)		-88	-87	dBm
12Mbps (FER≦10%)		-86	-79	dBm
18Mbps (FER≦10%)		-85	-77	dBm
24Mbps (FER≦10%)		-82	-74	dBm
36Mbps (FER≦10%)		-79	-70	dBm
48Mbps (FER≦10%)		-75	-66	dBm
54Mbps (FER≦10%)		-72	-65	dBm
Maximum Input Level (FER≦10%)	-20			dBm

3.8.4. IEEE802.11n 20MHz bandwidth mode

Item	Specification
Modulation Type	MIMO-OFDM
Channel	CH1 to CH14
Data rate	MCS0/1/2/3/4/5/6/7

TX Characteristics	Min.	Typical	Max.	Unit
Transmitter Output Power				
11n HT20Target Power		14.5		dBm
Spectrum Mask @ target power				
fc +/-11MHz			-20	dBr
fc +/-20MHz			-28	dBr
fc > +/-30MHz			-45	dBr
Frequency Error	-25	-1.2	+ 25	ppm
Constellation Error(peak EVM)@ target power				
MCS0			-5	dBm
MCS1			-10	dBm
MCS2			-13	dBm
MCS3			-16	dBm
MCS4			-19	dBm
MCS5			-22	dBm
MCS6			-25	dBm
MCS7		-32	-28	dBm
Transmit spectrum mask				
@ 11MHz			-20	dBr
@ 20MHz			-28	dBr
@ 30MHz			-40	dBr

RX Characteristics	Min.	Typical	Max.	Unit
Minimum Input Level Sensitivity				
MCS0 (FER≦10%)		-89	-82	dBm
MCS1 (FER≦10%)		-86	-79	dBm
MCS2 (FER≦10%)		-84	-77	dBm

RX Characteristics	Min.	Typical	Max.	Unit
MCS3 (FER≦10%)		-82	-74	dBm
MCS4 (FER≦10%)		-78	-70	dBm
MCS5 (FER≦10%)		-74	-66	dBm
MCS6 (FER≦10%)		-72	-65	dBm
MCS7 (FER≦10%)		-69	-64	dBm
Maximum Input Level (FER≦10%)	-20			dBm

3.9. Mechanical Dimensions

3.9.1. Core1081 Mechanical Dimensions

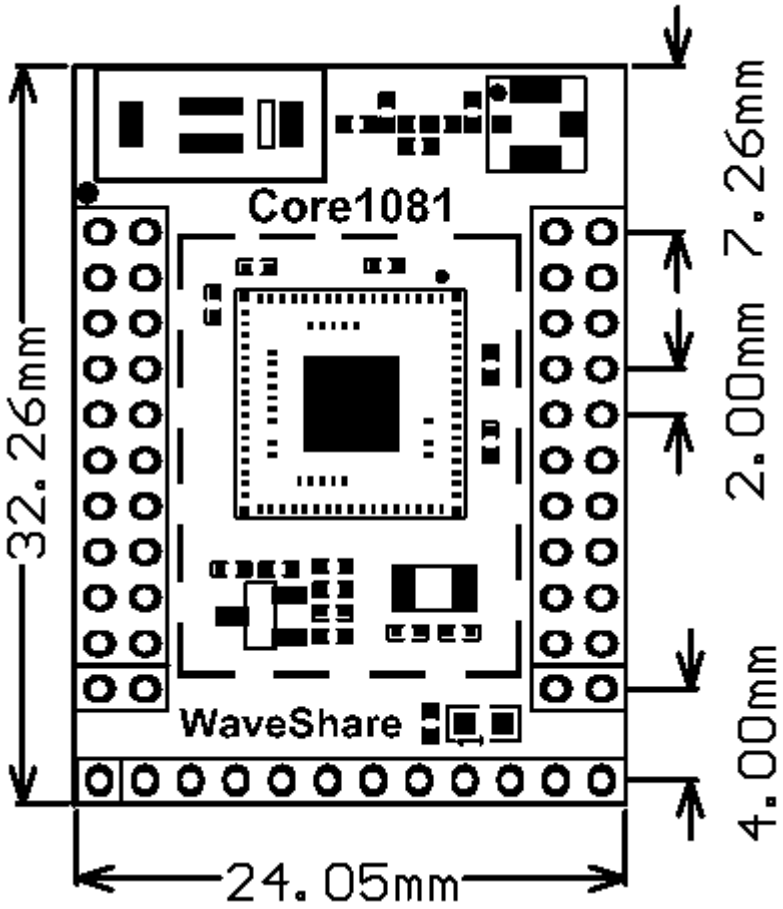
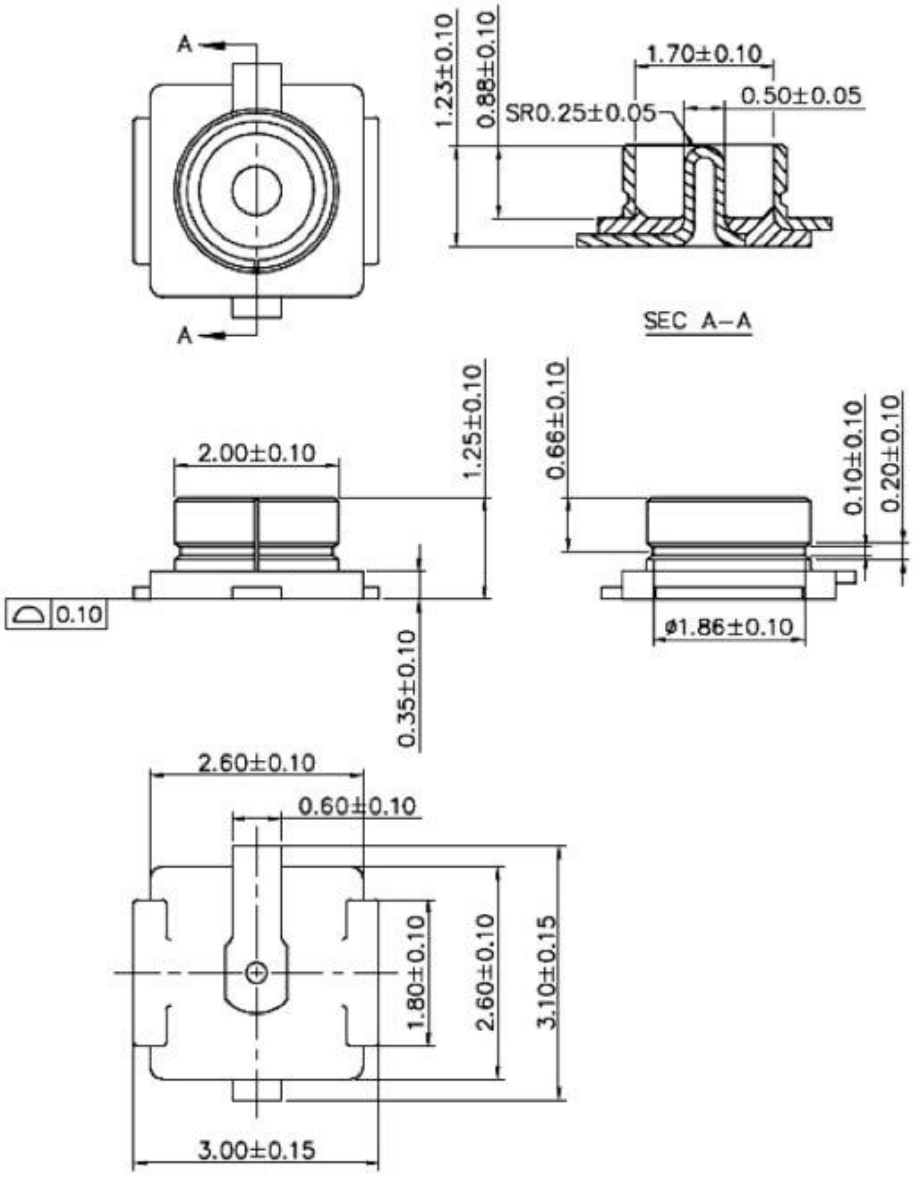


Figure3.1 Core1081 top view (Metric units)

4. Minimizing radio interference

4.1. U.F.L RF Connector

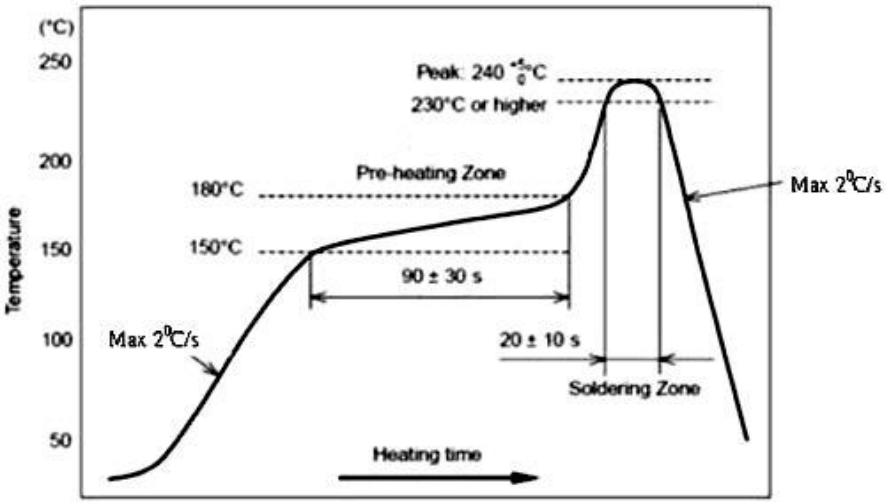
This module use U.F.L type RF connector for external antenna connection.



5. U.F.L RF Connector

5.1. Recommended Reflow Profile

Reflow times<= 2times (Max.)



Temperature profile for evaluation of solder heat resistance of a component (at solder joint)

5.2. MSL/Storage Condition

CAUTION

This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL 3

If Blank, see adjacent bar code label

1. Calculated shelf life in sealed bag: 12 months at < 40°C and < 90% relative humidity (RH)
2. Peak package body temperature: 260 °C
   If Blank, see adjacent bar code label
3. After bag is opened, devices that will be subjected to reflow solder or other high temperature process must
   a) Mounted within: 168 hrs. of factory conditions
      If Blank, see adjacent bar code label
      ≤ 30°C/60%RH, OR
   b) Stored at <10% RH
4. Devices require bake, before mounting, if:
   a) Humidity Indicator Card is > 10% when read at 23 ± 5°C
   b) 3a or 3b not met.
5. If baking is required, devices may be baked for 48 hrs. at 125 ± 5°C

   Note: If device containers cannot be subjected to high temperature or shorter bake times are desired, reference IPC/JEDEC J-STD-033 for bake procedure

Bag Seal Date: _____
If Blank, see adjacent bar code label

Note: Level and body temperature defined by IPC/JEDEC J-STD-020